Investigations of Solder Ball Drop Reliability: BGA versus WLP

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Abstract

In this paper, finite element modeling is performed to investigate the mechanisms ofreliability performance for wafer level packages (WLP) compared to chip scale ball grid array (BGA) packagesunder impact or drop loading conditions. Several scenarios are defined to reveal the different mechanisms of dynamic performance in WLP and BGA packages. Global/local finite element modeling is performed with the use of the direct acceleration input (DAI) method. In the first scenario of the simulation, a WLP (ball on I/O) package is compared to a BGA package with same ball geometries when package size is fixed. The vertical compliance at the package corner balls in BGA, due to the corner ball attachment to the compliant substrate/mold compound, makes BGA producing significantly less stresses than in WLP. However, when considering the second scenario, in which the same die is packaged with BGA and WLP (ball on I/O), respectively,the size of the package in BGA has increased, which presents the opposite effect in reducing the solder ball drop reliability. In the third scenario, a copper post WLP package is studied. It is found that the horizontal compliance by the epoxy layer, which is used to encapsulate the copper posts, has released the stresses in solder balls greatly under impact loading. Package size, vertical local compliance in BGA, and the horizontal compliance in WLP, constitute the major factors in determining the reliability performance of final products. Therefore, in the last scenario, a same device is packaged with a copper post WLP and a BGA, respectively. It is found the drop performance of a WLP is comparable to a BGA package. Wafer level packages are demonstrated to have comparable or even better drop performance than a BGA package. Existing experimental data show excellent agreement with the findings and observations in this study.

1. Introduction

Wafer level packages (WLP) and chip-scale ball grid array (BGA) packages are two major packaging options for low pin-count electronic devices in handheld applications due to the small-form factors.Conventional (fan-in) WLPs are formed on the dies while they are still on the uncut wafer (Fan, et al., 2008, 2009, 2010). The process can be thought of as an extension of front-end manufacturing in that it involves the entire wafer, but is more similar to bumping processes for flip chip packages. The final packaged device is the same size as the die itself. Thus, WLPs are a unique form of packages and have the distinction of being truly die- ip

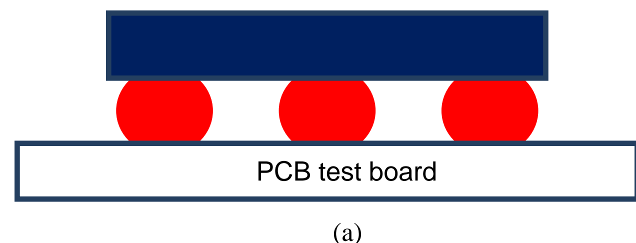
on I/O WLP, and copper post WLP etc (Fan, et al., 2010). In parallel, chip-scale BGA packages usually apply for wire-bonded dies in an area array format. The ratio of package/die size for a chip-scale BGA package is usually less than 1.2.

Drop and impact reliability of WLP and BGA packagesin handheld device applications is a major concern in electronics industry. Numerous data have been reported, based on both experimental tests and numerical simulations, on solder ball reliability under impact loading for chip scale BGA packages and WLPs. (Dhiman, et al, 2008a, b, 2009; Ranouta, et al., 2009; Irving, et al., 2004; Luan, et al., 2004; Lall, et al., 2006, 2007; Loh, et al., 2005; Park, et al., 2007; Ren, et al., 2003, 2004); Syed, et al., 2005; Tee, et all., 2004, 2008; Wong, et al., 2003; Zhu, et al., 2003). However, little study has been conducted to compare the reliability performance for a BGA package versus a WLP package. The lack of the understanding for BGA vs. WLP is probably due to the fact that there areso many variations in geometries and materials that it is difficult to have a single straightforward comparison.

In this paper, finite element modeling is performed to investigate the mechanisms of reliability performance for WLPs compared to chip scale BGA packagesunder impact or drop loading conditions. Several scenarios are defined to investigate the solder ball drop reliability for both packages. The conflicting mechanisms are reveled and decoupled by different scenarios. The combined effects are then considered for a same device (die size) packaged with WLP and BGA respectively. The comparison with exiting experimental data is discussed.

2. Simulation Scenarios

There are many variations in layout, geometry, and materials between WLP and BGA packages. In this study, several scenarios are defined to decouple those contributing factors. In the first scenario, it is assumed that the BGA package size is same as a WLP size with same ball geometry and ball pitch, as shown in Figure 1. This implies that the die size of the BGA package is smaller than the WLP die. In this scenario, ball on I/O WLP structure is applied. The goalis to investigate the effect of packaging format for the same package size on the reliability performance under impact.



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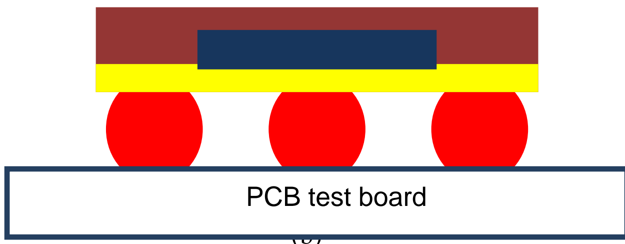


Figure 1 Scenario 1: ball on I/O WLP vs. chip scale BGA package (package size fixed): (a) ball on I/O WLP; and (b) chip scale BGA package

In the second scenario, die size is fixed. Ball on I/O WLP structure is compared to a BGA package with a same die, as shown in Figure 2. This scenario provides a direct comparison for a same die with two different packaging options.

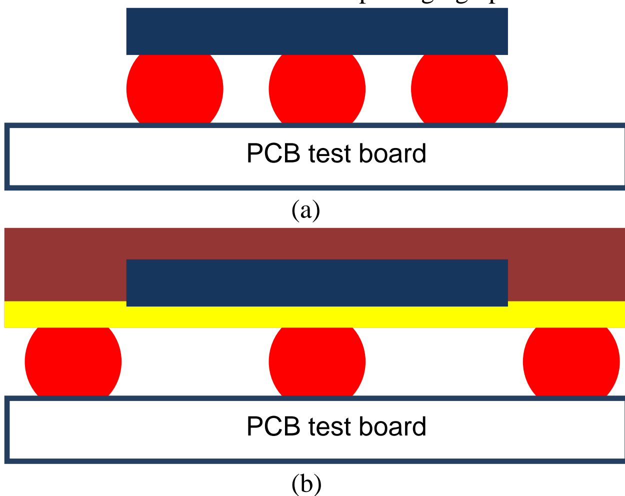
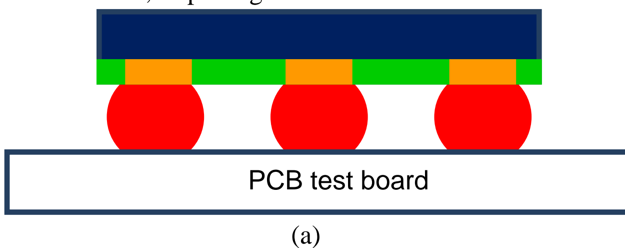


Figure 2 Scenario 2: ball on I/O WLP vs. chip scale BGA package (die size fixed): (a) ball on I/O WLP; and (b) chip scale BGA package

As ball on I/O WLP structure has now been rarely used in real applications, in the third scenario, a copper post WLP structure is considered, as shown in Figure 3. In this case, the solder balls are connected to thick copper posts, which are encapsulated by epoxy at wafer level. When the modulus of epoxy is assumed to be as rigid as silicon, the copper post WLP will be structurally similar to the ball on I/O WLP in scenarios 1 and 2 (to be verified through modeling).Therefore, the results with different modulus of epoxy for a copper post WLP can then be compared to a BGA package, either with same die size, or package size.



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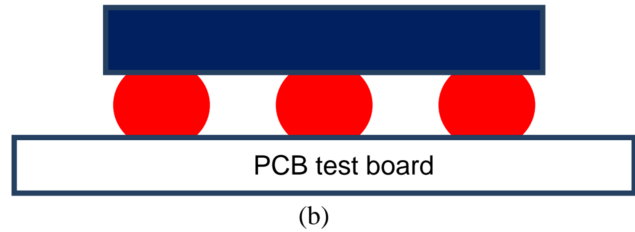

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Figure 3 Scenario 3:copper post WLP vs. ball on I/O WLP: (a) copper post WLP; and (b) ball on I/O WLP

In the last scenario, the device size is same, but with two options to package with either a copper post WLP or a BGA package. The BGA package will have a larger package size than WLP. The comparison of the drop reliability performance is studied and compared with the experimental data.

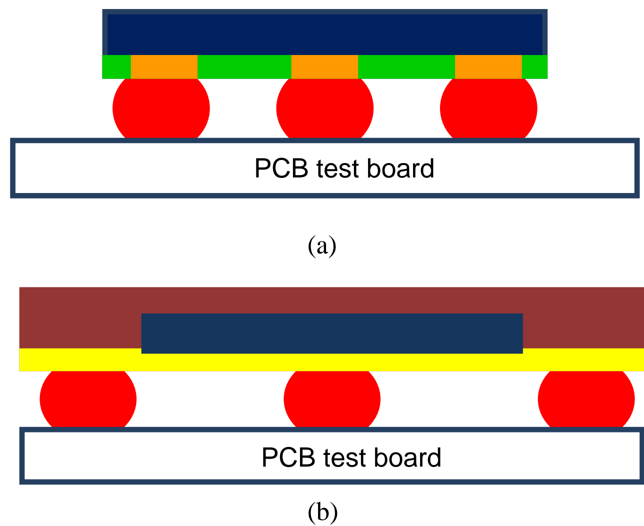


Figure 4 Scenario 4:copper post WLP vs. chip scale BGA: (a) copper post WLP; and (b) chip scale BGA

3. Finite Element Modeling

There are 15 components on a JEDEC-specified drop test board, and each component has hundreds of solder balls. Inperforming finite element analysis,special treatmentsmust bemade in both global and local model levelsto handle this very large model without the sacrifice of accuracy. In the global model, a quarter JEDEC board is used. Solder balls in global model are simplified asrectangular blocks with one 3-D solid element for each ball, as shown in Figure 5. A local model is developed at any desired location of the components in test board. Figure 6 shows an example of a local model for component U1 (corner components as defined in JEDEC standard). In the local model, the board is extended to 2mm away from the component corner in both x and y directions, respectively to create cut boundary and DOF constraints taken from global model. All solder balls in the local model are modeled as rectangular blocks, except critical solder ball(s) with refined meshes and detailed structures. Since the primary failure is at the intermetallic layer on package side, a 10 μm

layer with two layers of elements is created at solder ball upper interface. 3-D solid elements are used for the entire structure including PCB board. Direct acceleration input (DAI) method is used to apply impulse loading (Dhiman, et al, 2008a, b, 2009). The damping coefficient for PCB is determined by correlating with experimental strain data.

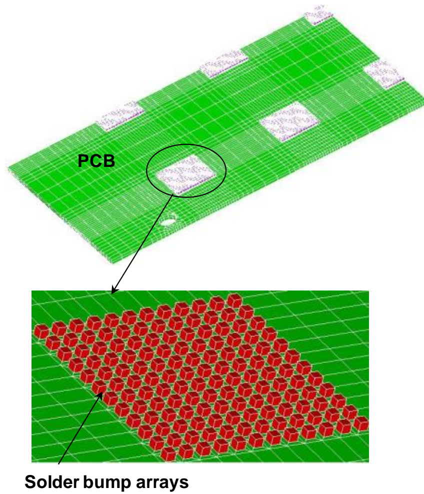
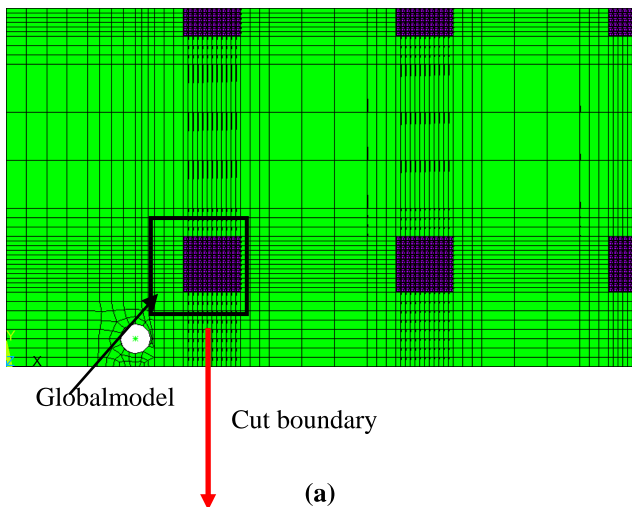


Figure 5 A quarter global finite element model

Table 1 defines the material properties used for both global and local finite element models. All the materials are considered as elastic ones.

Table 1Material Properties

Material	Mechanical Properties		
	Modulus (GPa)	Poisson Ratio	Density (gm/cm^3)
PCB	22	0.25	2.1
Solder (SAC)	51	0.36	7.2
Silicon Die	130	0.278	2.5
Underfill	10	0.3	2.0
Copper Post	128.8	0.34	8.3
Epoxy	4.7	0.38	2.2
Passivation	2.89	0.34	2.2
PCB Pad	128.8	0.34	8.3



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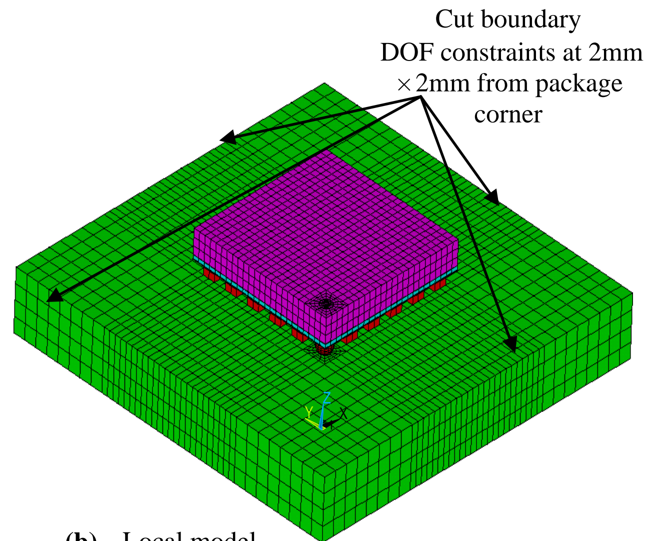
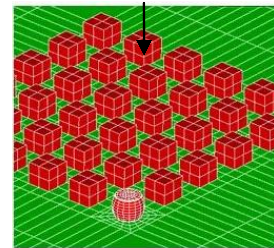


(b) Local model



(c) Solder ball meshes in local model

Figure 6local finite element models(**a**). cut boundary from global model; (**b**). 3-D view of a local model; (**c**).solderball meshes in the local model

4. Results and Discussions

4.1 Scenario 1

Previous studies have shown that for any components located on the JEDEC test board, the maximum peeling stresses in each component always occur at package corners. (Ranouta, et al., 2009).Thus, in this study, only corner balls in two packages are investigated. The component U1 on the JEDEC test board is selected. Figure 7 shows the maximum peeling stress during drop for a WLP vs. BGA. From Figure 8, it can be seen that the corner balls in BGA are connected to interposer (substrate)/mold compound (8(b)), which provides a local flexibility in vertical movement for corner balls. However, in a ball on I/O WLP package, the solder balls are

to the peeling stress in BGA corner balls significantly lower than that in WLP, as shown in Figure 7.Local compliant structure of substrate/mold compoundis connected to the solder balls in a vertical direction at package corners in BGA to provide a mechanism as spring structure to release the stresses in solder balls.

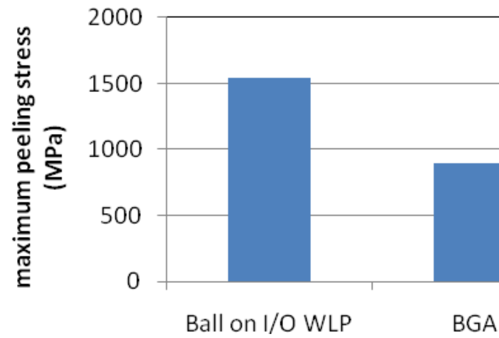


Figure 7 maximum peeling stresses for corner balls in U1 for scenario 1

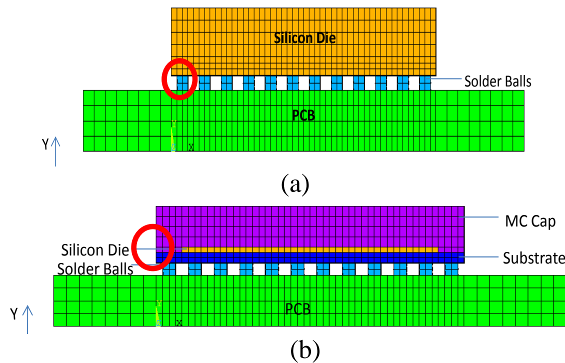


Figure 8 Corner solder ball attachment in (a) ball on I/O WLP, and (b) chip scale BGA package

4.2Scenario 2

Many simulation and experimental data have been reported that the package size plays a significant role in affecting solder ball drop reliability. The greater the package size is, the less the reliability of solder balls is subjected to impact (Ranouta, et al., 2009). For a same die, if the WLP packaging is selected, the package size is the same of the die size. If the BGA packaging is selected, the package size will be greater. Assuming that the package size is 1.2 times of die size, it can be seen that two opposite mechanisms exist in BGA packages: larger package size will decrease the solder ball reliability, while corner solder balls in a BGA benefit from the local compliance as illustrated in the scenario 1. Figure 9 shows the simulation results of the maximum peeling stresses for scenario 2. Compared to the scenario 1, ball stresses in BGA has increased considerably due to the increase of package size.

Figure 9maximum peeling stresses for corner balls in U1 for scenario 2

4.3Scenario 3

Ball on I/O WLP package is used in scenarios 1 and 2. However, such a WLP structure has been rarely used now (Fan, et al. 2010). Among a variety of WLP packages, copper post WLP package has shown the superior reliability performance in thermal-mechanical reliability (Rahim, et al., 2009; Zhou, et al., 2009). In a copper post WLP, thick copper pillars (~70 μm) are electroplated, followed by an epoxy encapsulation at wafer level. The copper post WLP can also incorporate with redistribution layer (RDL). The epoxy used in copper post WLP is very compliant with a typical modulus of 5 to 20 GPa, which is only a fraction of the modulus of silicon die (130GPa). Table 2 shows the results of a parametric study of the maximum peeling stress as a function of epoxy modulus, compared to a ball on I/O WLP. As expected, when the epoxy modulus approaches the modulus of silicon, the peeling stress is very close to the stress in balls on I/O WLP. With the decreasing of the epoxy modulus, the solder ball stresses can be reduced greatly. For the epoxy modulus of 4.7MPa, the stress in a copper post WLP is much less than the stresses in BGA for a same package size as shown in scenarios 1, and for the same die in scenario 2, respectively.Table 2 clearly shows the beneficial results of the drop performance for a copper post WLP, due to the compliance of the epoxy modulus. Such an epoxy/copper post layer structure may be viewed as a horizontal spring structure to release the stresses in solder balls greatly.

Table 2 maximum peeling stress as function of epoxy modulus in copper post WLP

Epoxy modulus (GPa)	4.7	14	20	130	Ball on I/O WLP
Maximum peeling stress (MPa)	539.1	821.8	942.5	1610	1538.3

4.4Scenario 4

There are three mechanisms revealed from the above analysis for each scenario: package size, vertical local compliance by substrate/mold compound in BGA, and the horizontal compliance by epoxy in copper post WLP. The actual performance of a WLP versus a BGA will depend on the combined effects of those three factors.In the last scenario, the same device (die) is considered with two packaging options: copper post WLP, and chip scale BGA package. The BGA package will have larger package size than the WLP.There are three competing mechanisms that will affect the drop reliability of both packages. For the BGA package, the increase of the package size will definitely decrease the drop performance. However, the local compliance for the outermost solder balls in a BGA will improve the solder ball drop reliability greatly. The selection of mold compound will affect the peeling stress in solder balls. On the other hand, for a copper post WLP package, the epoxy layer acts as a

horizontal spring structure to release the stresses in solder balls. Figure 10 plots the results of the maximum peeling stress for these two packages. For the given material properties for both packages, the stress level in both packages is comparable. This means that a copper post WLP package will have the drop reliability as good as a BGA package, or even better.

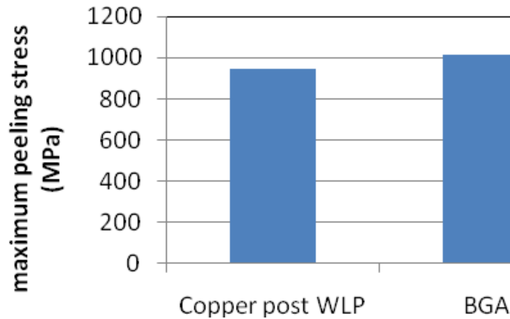


Figure 10 maximum peeling stresses in a BGA and a copper post WLP package (same die size)

Althoguh there are no direct experimental data available to validate the above results and findings, the individual resuts from several sources may support the conclusions made in this study. It has been known that BGA packages have acceptable drop performance with respect to the requirement of the JEDEC standard (Syed, et al. 2005). However, many experimental data for different types of WLP packages show the surprising superior reliability performance. For example, the number of drops for the WLP packages tested by Amkor acheives as high as more than 2000 drops (Tee, et al., 2009). Such observations are also confirmed by the experimental work of the authors (Ranouta, et al. 2009). This illustrates that the smaller size of WLP, together with the compliant layer between the solder balls and dies, improve the WLP reliability under impact loading signifcantly.

5. Conclusions

In this study, the fundamental mechanisms associated with chip scale BGA packages and wafer level packages are investigated. For a BGA package, the package size may be greater than a WLP package. Therefore the solder ball reliability is compromised. However, the corner solder balls, which are attached to the interposer (substrate) and mold compound, benefit greatly from the local vertical compliance generated by substrate/mold compound structure. Therefore, the solder ball stresses at the package corner can be reduced in a great deal. For a WLP package, if the solder balls are attached to silicon directly, such as in a ball on I/O WLP, the solder balls will have greater risk in drop performance. For a copper post WLP, or ball on polymer WLP, the compliant layer between solder balls and die act as a horizontal spring structure to absorb the stresses in solder balls. This will improve the WLP solder ball reliability greatly. In summary, the drop performance of a WLP is comparable to a BGA package. Wafer level packages are demonstrated to have comparable or even better drop performance than a BGA package.

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